

- 1(a) Ben installs burglar alarms. The alarm is made up of a door sensor and a motion sensor. When the alarm is set, the siren will sound if either the door sensor or the motion sensor detect movement.

The alarm also has a test mode setting. When the test mode setting is enabled, an engineer can check the sensors are working without the siren going off.

The inputs to the alarm are as follows.

Input	System
A	Door sensor
B	Motion sensor
C	Alarm has been set
D	Test mode enabled

Draw a logic circuit to show the logic that is used in the burglar alarm to determine if the siren goes off.



[4]

(b)

- i. Simplify the Boolean expression $\neg A \vee \neg B$ using De Morgan's First Law.

----- [1]

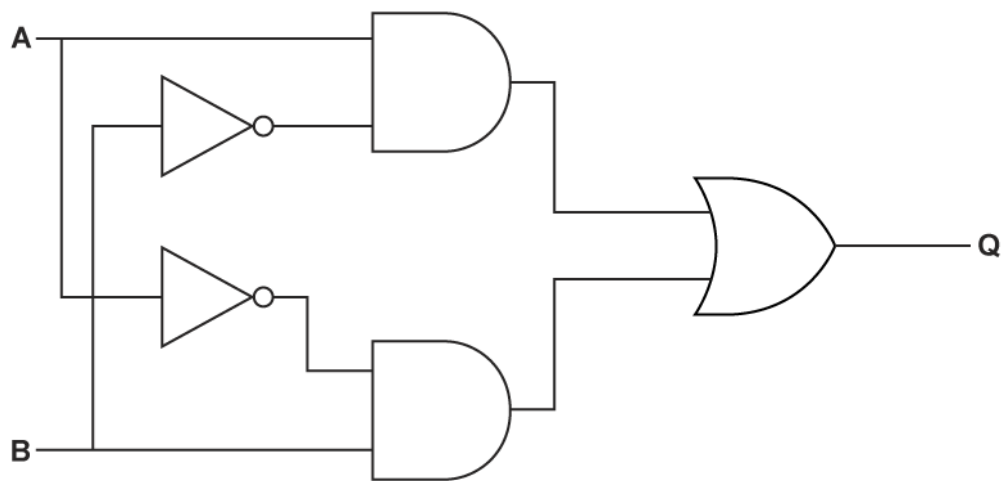
- ii. Simplify the Boolean expression $\neg(\neg B)$ using double negation.

----- [1]

- iii. Simplify the Boolean expression $(A \vee B) \wedge (A \vee C)$ using distribution.

----- [2]

2(a) A logic gate diagram is shown below.



i. Complete the truth table for this logic gate diagram.

A	B	Q
0	0	
0	1	
1	0	
1	1	

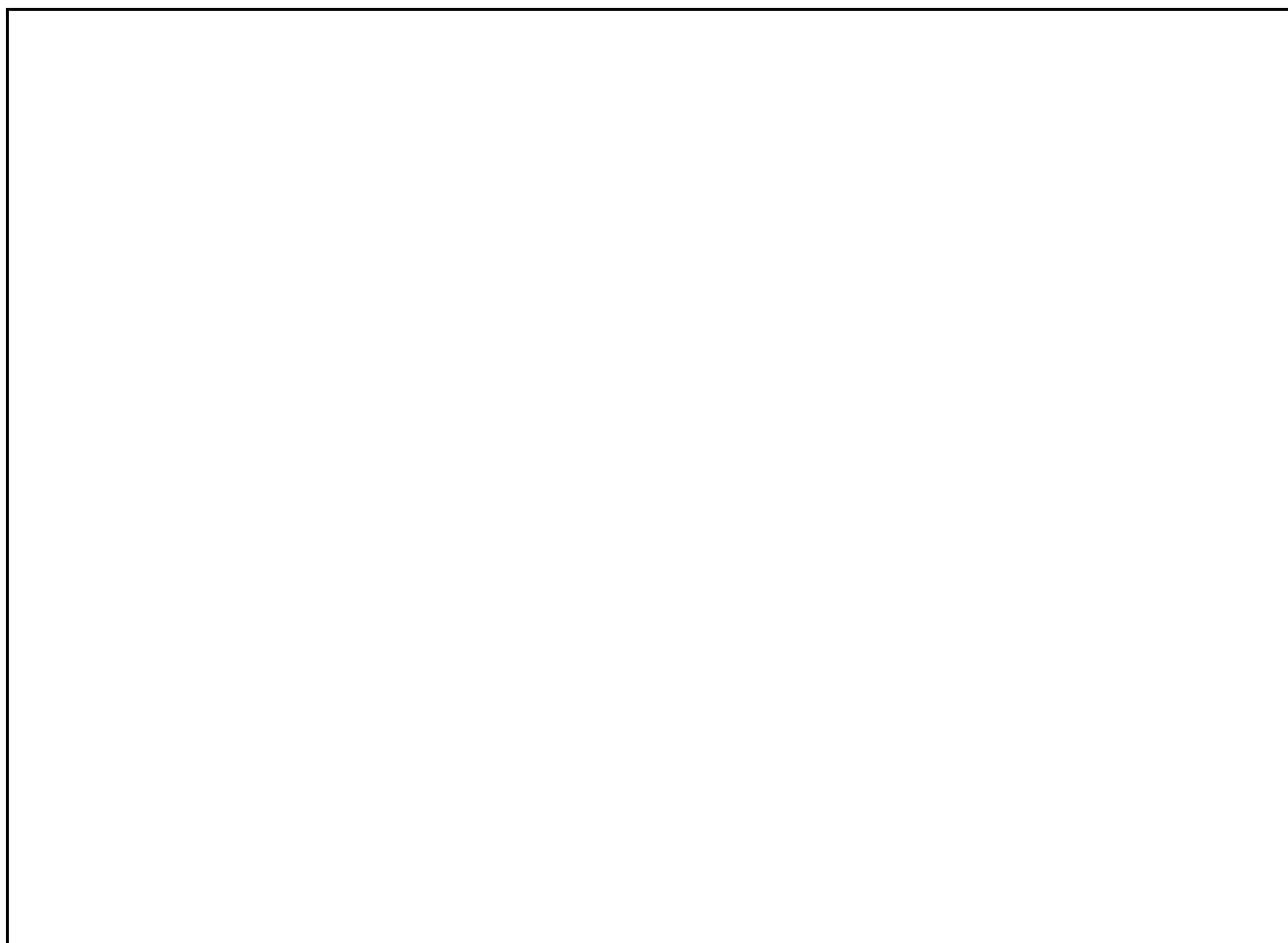
[2]

ii. What single gate is this logic gate diagram equivalent to?

[1]

(b) Draw the logic gate diagram for this expression:

$$Q = (A \vee \neg B) \wedge C$$



[3]

3(a)

A computer scientist has created the following logic circuit shown in Fig. 6.

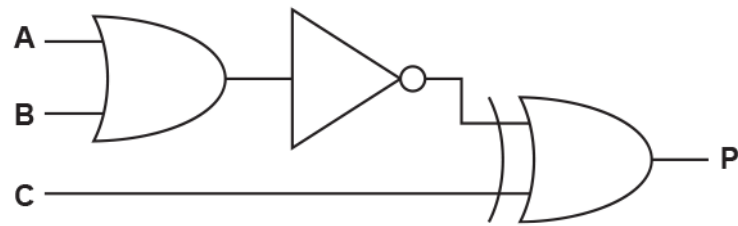


Fig. 6

- i. Give the Boolean expression that represents the logic circuit shown in Fig. 6. Do not attempt to simplify the expression.

[2]

- ii. Complete the truth table for the logic circuit shown in Fig. 6.

A	B	C	P
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[3]

(b) The following Karnaugh map represents another logic circuit.

		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	1	1	0	0
	11	0	0	0	0
	10	0	0	1	1

Use this Karnaugh map to find the simplified expression for this circuit.

You should highlight the map as appropriate and write the expression here.

[4]

4(a) Elliott has designed a logic circuit. The expression he has created for the logic circuit is:

$$Q = (A \wedge \neg B) \vee (\neg A \wedge C \wedge D) \vee (A \wedge B)$$

Complete the Karnaugh Map below to simplify this expression. Show your working.

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

Simplified expression:

[4]

(b) Draw a Logic diagram for the following expression:

$$Q = \neg(A \wedge B) \vee (C \wedge \neg D)$$



[3]

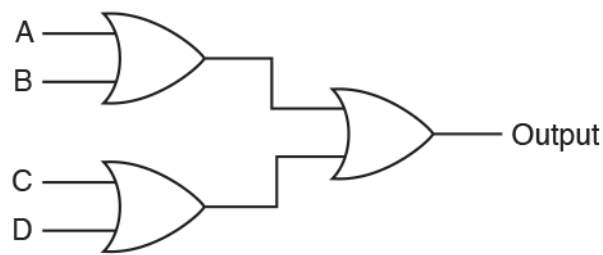
5(a) Draw an XOR gate.

[1]

(b) Explain the difference in the function of OR and XOR gates.

[2]

(c) A circuit contains the logic gates shown below.



i. Complete the logic table below.

A	B	C	D	Output
1	1	1	1	
1	1	1	0	
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	
0	0	0	0	

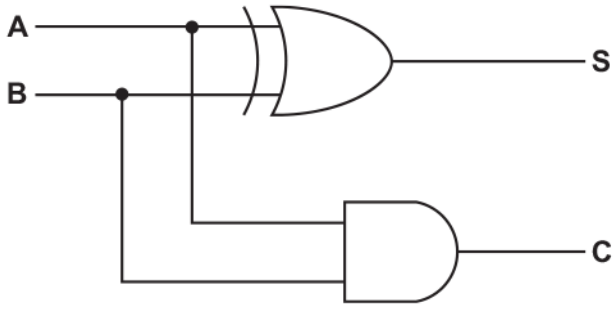
[4]

ii. Complete the Boolean expression below to represent the circuit.

----- $\equiv$ Output

[2]

6(a)



The logic circuit above has two inputs (A, B) and two outputs (S, C).

- i. Give the Boolean expressions for the outputs S and C.

S ≡ _____

C ≡ _____

[2]

- ii. Complete the truth table for this logic circuit.

A	B	S	C
0	0		
0	1		
1	0		
1	1		

- iii. Describe how this logic circuit can be adapted to add together two 4-bit binary numbers.

[4]

[4]

- (b) All users of a computer system have a unique username and password. The computer system has implemented two-factor authentication so that users must respond to either an email or text message containing a secret code to be able to access the system.

Let:

A be a Boolean value for if a user enters a valid username

B be a Boolean value for if a user enters a password that matches their username

C be a Boolean value for if a user is able to respond to an email containing a secret code

D be a Boolean value for if a user is able to respond to a text message containing a secret code

Q be a Boolean value for if entry to the computer system is allowed

Complete the Boolean expression below:

$Q \equiv$

- (c) Another Boolean expression for a logic system is shown below:

$$Q \equiv \neg (\neg A \wedge \neg B)$$

- i. Simplify this Boolean expression so that it does not include any negation. You must explain which Boolean algebra rule(s) you are using at each step.

.....

.....

.....

.....

[2]

7(a)

i. Complete the Karnaugh map below for the Boolean expression $(\neg A \wedge \neg B) \vee (A \wedge \neg B)$

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

[3]

ii. Use the Karnaugh map to find a simplified Boolean expression that is equivalent to $(\neg A \wedge \neg B) \vee (A \wedge \neg B)$

[2]

(b)

i. State the purpose of a D-type flip-flop circuit.

----- [2]

ii. Describe the inputs and outputs used by a D-type flip-flop circuit, explaining how the inputs are used to control the outputs.

----- [4]

8 Daniel is an engineer. He has created the following logic circuit shown in Fig. 4.

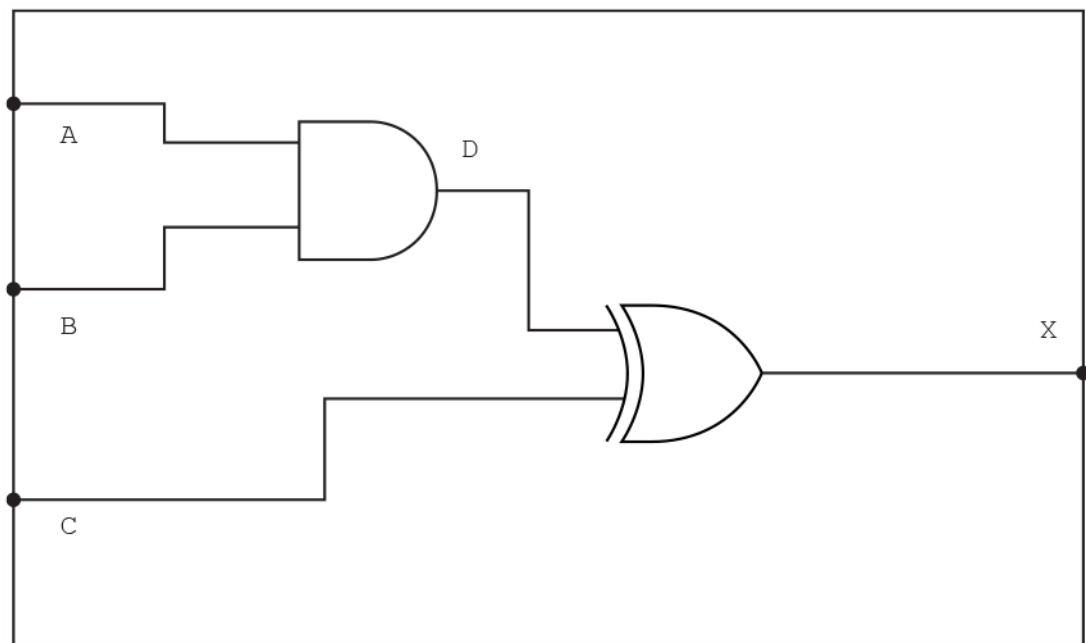


Fig. 4

Complete the truth table below for the logic circuit shown in Fig. 4.

A	B	C	D	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[4]

9 A company releases an in-home virtual assistant called 'Bertie Butler'.

The device, when placed in a room, listens out for the phrase "Hey Bertie". When someone says that phrase it then listens to the question that follows and tries to give a relevant answer.

Bertie Butler has a number of built-in input and output devices.

Bertie Butler's circuitry is designed to only listen out for "Hey Bertie" under certain circumstances, which are:

The privacy button (**P**) must be off and the microphone must generate a signal (**S**) to say a sound has been heard.

i. Complete the truth table for whether the device is listening (**L**).

P	S	L
False	False	
False	True	
True	False	
True	True	

[2]

ii. Draw logic gates to represent the circuitry needed.

[3]

10 Complete the truth table to represent the following Boolean expression.

$$Q \equiv \neg (A \wedge B) \vee C$$

A	B	C	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[2]

11(a)

Draw a logic gate diagram to represent the Boolean expression

$$Q \equiv \neg A \vee B$$

[2]

(b) Find the Boolean expression represented in the Karnaugh Map below. Show your working.

		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	0	0	1	1
	11	0	0	0	1
	10	0	0	0	1

[5]

12(a) A cinema offers discounted tickets, but only under one of the following conditions:

- Customer is under 18 and has a student card.
- Customer is over 60 and has ID which proves this.

Let:

A be Customer is under 18

B be Customer has a student card

C be Customer is over 60

D be Customer has ID

Q be Discount ticket issued

Complete the Boolean expression below:

Q ≡ _____ [3]

(b) The cinema has a voucher which promises free popcorn when the voucher is produced whilst buying a soft drink or bottle of water.

Let:

E be Voucher is shown

F be Soft drink is bought

G be Bottle of water is bought

R be Free popcorn given.

This could be written as:

$$R \equiv (E \wedge F) \vee (E \wedge G)$$

i. Complete the truth table below.

E	F	G	$(E \wedge F)$	$(E \wedge G)$	$(E \wedge F) \vee (E \wedge G)$
1	1	1			
1	1	0			
1	0	1			
1	0	0			
0	1	1			
0	1	0			
0	0	1			
0	0	0			

[4]

ii. Simplify the expression

$$(E \wedge F) \vee (E \wedge G)$$

----- [2]

Most films are now distributed to cinemas digitally. A studio allows cinemas to download its latest film 5 days before the release date via a private download. It wants to ensure that no cinema shows it before the release date.

13(a) A half adder has the truth table shown below:

A	B	Sum	Carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

Draw a half adder using logic gates.

[3]

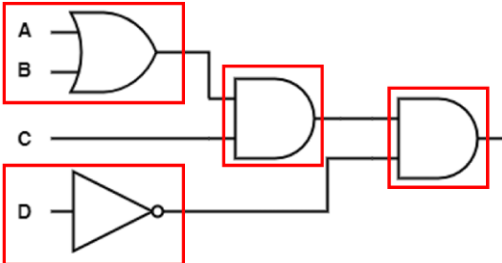
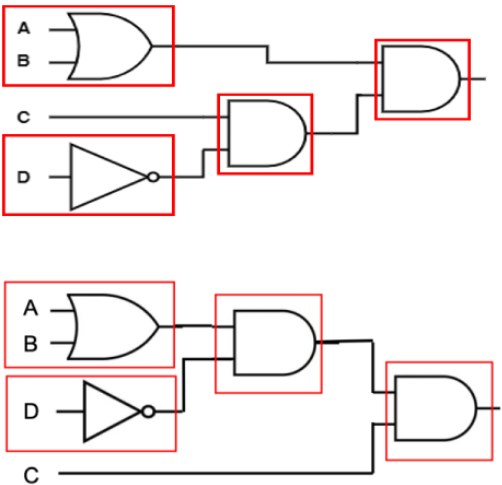
(b) Draw the logic gates represented by the Karnaugh Map below. Show your working.

		AB			
		00	01	11	10
CD	00	1	1	0	0
	01	1	1	0	0
	11	0	0	1	1
	10	0	0	1	1

[4]

END OF QUESTION PAPER

Mark Scheme

Question	Answer/Indicative content	Marks	Guidance
1 a	1 mark for each correct area including labelled inputs  Alternatives (1 mark per area): 	4	Max 3 if any additional gates. NOT gate must have only one input, AND/OR gates must have two inputs NOT gate must have circle Ignore any names on gates Examiner's Comments There were a range of marks on this question. More successful candidates gave all four gates accurately, but most candidates were able to gain at least one or two marks. Some candidates were unaware of what a logic circuit was and instead produced a range of different diagrams including flow charts.
b i	$\neg (A \wedge B)$	1	Accept NOT (A AND B) / other correct notations e.g. $\overline{A.B}$ $\neg$ must be the correct way round Examiner's Comments Many candidates gained full marks with the most common error being $\neg(A \vee B)$
ii	B	1	Examiner's Comments Almost all candidates were able to gain a mark on this question.

Mark Scheme

Question			Answer/Indicative content	Marks	Guidance															
		iii	1 mark for A 1 mark for $\vee (B \wedge C)$ $A \vee (B \wedge C)$	2	Doesn't need brackets Allow other correct notation e.g. $A+B.C$ Allow either order e.g. $(B\wedge C) \vee A$ Allow $A\vee(BC)$ / $A\vee BC$ <u>Examiner's Comments</u> The majority of candidates recognised that distribution meant that there was only one A following simplification but the most common error for the second mark was again to use OR instead of AND for B AND C															
			Total	8																
2	a	i	<table border="1"><tr><td>A</td><td>B</td><td>Q</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> 1 Mark for the first 2 rows 1 mark for the last 2 rows	A	B	Q	0	0	0	0	1	1	1	0	1	1	1	0	AO2.2 (2)	<u>Examiner's Comments</u> The majority of candidates were able to correctly complete the truth table for both marks.
A	B	Q																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	0																		
		ii	XOR	AO1.2 (1)	Accept "Exclusive OR" <u>Examiner's Comments</u> Most candidates correctly stated the correct single logic gate (XOR).															
	b		 - A going into an OR gate - B going into a NOT gate with the output going into the OR gate - Output of the OR gate going into an AND gate with C	AO3.1 (3)	<u>Examiner's Comments</u> Most candidates were able to draw the three logic gates correctly, although some did not make it clear the difference between an 'and' gate and an 'or' gate in their diagram.															
			Total	6																

Mark Scheme

Question			Answer/Indicative content	Marks	Guidance																																								
3	a	i	• $\neg (A \vee B)$ // NOT (A OR B) • $\underline{\vee} C$ // XOR C	2	First MP requires brackets, NOT A or B is incorrect. Can be written in different order (e.g. C XOR NOT (B OR A) as long as logically correct. Accept $(A + B) \oplus C$ <u>Examiner's Comments</u> This question was generally well answered, although some candidates confused AND and OR																																								
		ii	• 1 mark for first two rows (1,0) • 1 mark for next two rows (0,1) • 1 mark for next four rows (0,1,0,1) <table><tr><th>A</th><th>B</th><th>C</th><th>P</th><th>Marking Guidance</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">1 Mark</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="2">1 Mark</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="4">1 Mark</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	A	B	C	P	Marking Guidance	0	0	0	1	1 Mark	0	0	1	0	0	1	0	0	1 Mark	0	1	1	1	1	0	0	0	1 Mark	1	0	1	1	1	1	0	0	1	1	1	1	3	<u>Examiner's Comments</u> This question was generally well answered.
A	B	C	P	Marking Guidance																																									
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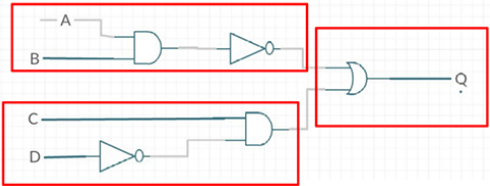
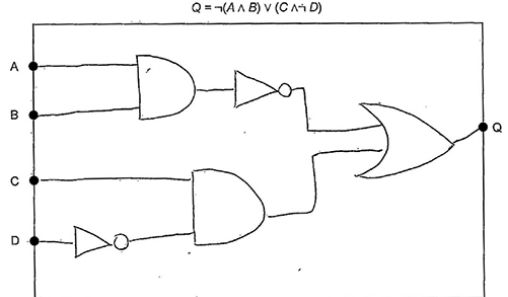
Mark Scheme

Question			Answer/Indicative content	Marks	Guidance
	b		• Correct highlighting on K map as shown • $\neg A \wedge \neg C // \bar{A}.\bar{C} // \text{NOT A AND NOT C...}$ • $A \wedge \neg D // A.\bar{D} // \text{A AND NOT D...}$ • $\dots \vee // + // \text{OR joining the 2 correct expressions together}$	4	AB 00011110 0011 11 10 0011 01 11 10 Do not penalise candidates who attempt to simplify even further (e.g. NOT A AND NOT C = NOT (A OR C) using De Morgan's). MP1 - correct answer only MP4 is dependent on MP2 & 3 <u>Examiner's Comments</u> There were many candidates who were able to gain full marks on this question. Those who did not showed a lack of understanding of grouping on a Karnaugh map, either grouping to include zeros or missing the wrapping group and adding another group in for the top row.
			Total	9	

Mark Scheme

Question		Answer/Indicative content	Marks	Guidance																																				
4	a	Solution: <table border="1"><tr><td></td><td></td><td>AB</td><td>AB</td><td>AB</td><td>AB</td></tr><tr><td></td><td></td><td>00</td><td>01</td><td>11</td><td>10</td></tr><tr><td>CD</td><td>00</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>CD</td><td>01</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>CD</td><td>11</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>CD</td><td>10</td><td>0</td><td>0</td><td>1</td><td>1</td></tr></table> 1 mark per bullet up to a maximum of 4 marks: • 1 mark for filling in the table correctly • 1 mark for the group shown in red • 1 mark for the group shown in green • 1 mark for the simplified expression $A \vee (C \wedge D)$			AB	AB	AB	AB			00	01	11	10	CD	00	0	0	1	1	CD	01	0	0	1	1	CD	11	1	1	1	1	CD	10	0	0	1	1	4 (AO2.1) (2) (AO2.2) (2)	Brackets are not required for the simplified expression Examiner's Comments This question was answered well with many candidates achieving all 4 marks. Some completed the table correctly but were not able to simplify the expression appropriately.
		AB	AB	AB	AB																																			
		00	01	11	10																																			
CD	00	0	0	1	1																																			
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CD	11	1	1	1	1																																			
CD	10	0	0	1	1																																			

Mark Scheme

Question	Answer/Indicative content	Marks	Guidance
b	 1 mark per bullet up to a maximum of 3 marks: • An AND gate taking A and B as inputs with the output connecting to a NOT gate • An AND gate taking C and the NOT of D as the inputs • An OR gate taking the outputs of the NOT and AND gates	3 (AO3.1) (3)	Allow NAND gate as alternative for BP1 Examiner's Comments As with the first part of this question, this was answered well. Most candidates used the same gates that are shown in the mark scheme, although equivalent gates were accepted. Some candidates lost marks for not being clear on the type of gate they had decided on. Exemplar 2  Exemplar 2 was given full marks. This candidate has gained all 3 marks as the gates are correct and are clearly drawn to avoid confusion. Each gate also has the correct number of inputs and outputs in all three instances. Logic gate guidance To make sure full credit is given for the answers provided, it is essential that the drawings are clear enough to distinguish one gate from another. Some gates look similar, so the lines and symbols need to be clear enough to establish which gate has been used.
	Total	7	

Mark Scheme

Question			Answer/Indicative content	Marks	Guidance																																																																																					
5	a			1 AO1.1	Accept diagram of gate only without input / output <u>Examiner's Comments</u> There were very few candidates who could not correctly draw an XOR gate.																																																																																					
	b		OR gate outputs true if at least one of its inputs is true (1) XOR gate output true if and only if one of its inputs is true. (1)	2 AO1.2	Accept appropriate, correctly labelled, truth tables. One mark for each truth table. <u>Examiner's Comments</u> A lack of clarity of expression led to candidates not gaining credit in this question. Some candidates who achieved full marks supported their descriptions with correct two-input truth tables which clearly demonstrated the difference.																																																																																					
	c	i	<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Output</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> 1 Mark 1 Mark 1 Mark 1 Mark	A	B	C	D	Output	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0	1	0	1	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	1	1	0	1	0	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	0	4 AO2.2	<u>Examiner's Comments</u> This question was well received by candidates with most achieving full marks.
A	B	C	D	Output																																																																																						
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		ii	(A ∨ B) ∨ (C ∨ D) ≡ Output A ∨ B (1 Mark) ∨ (C ∨ D) (1 Mark)	2 AO2.2	Accept answer without brackets. Accept alternative notation i.e. OR , + <u>Examiner's Comments</u> Boolean expressions were in the main correct. All standard notations was credited provided it was used consistently.																																																																																					
			Total	9																																																																																						

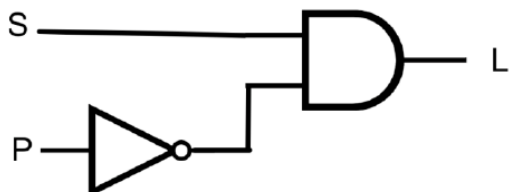
Mark Scheme

Question			Answer/Indicative content	Marks	Guidance																				
6	a	i	$S = A \vee B$ $C = A \wedge B$	2 AO2.1	Accept alternative symbols for AND /XOR																				
		ii	1 mark for S column 1 mark for C column	2 AO2.1	<table><tr><th>A</th><th>B</th><th>S</th><th>C</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr></table>	A	B	S	C	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	1
A	B	S	C																						
0	0	0	0																						
0	1	1	0																						
1	0	1	0																						
1	1	0	1																						
		iii	- Logic circuit adds together 2 binary digits / half adder - S gives sum, C gives carry - Two half adders can be joined together... ...with an OR gate - to form full adder 4 full adders can be used to add two four bit numbers - Carry out on one joined to carry in on next	4 AO1.2																					
	b		$Q \equiv A \wedge B$ $\wedge$ $(C \vee D)$	3 AO1.2	$Q \equiv A \wedge B \wedge (C \vee D)$ Accept alternative symbols for AND / OR e.g. $Q = A \text{ AND } B \text{ AND } (C \text{ OR } D)$ Brackets must be included for 3 rd point Allow XOR for bullet point 3 Any additional symbols max 2 marks																				
	c		- Identification of De Morgan's and/or double negation rule - Correct final answer to give $A \vee B$	2 AO2.2																					
			Total	13																					

Mark Scheme

Question			Answer/Indicative content	Marks	Guidance
7	a	i	• left column filled with 1s ($\neg A \wedge \neg B$) ... • right column filled with 1s ($A \wedge \neg B$)... • ...Middle 2 columns filled with zero or blank	3 AO1.2 (1) AO2.2 (2)	AB 00 01 11 10 CD 00 1 0 0 1 01 1 0 0 1 11 1 0 0 1 10 1 0 0 1
		ii	• $\neg B$ / NOT B • Karnaugh map used to show 1s highlighted with overlap	2 AO2.2	AB 00 01 11 10 CD 00 1 0 0 1 01 1 0 0 1 11 1 0 0 1 10 1 0 0 1
	b	i	• Delay / store a value... • ...of 1 bit • When a signal is given	2 AO1.1	
		ii	• Data input • Clock input • Q output • When clock input goes high... • ...Q changes to D • NOT Q is reverse of Q	4 AO1.1 (2) AO1.2 (2)	
			Total	11	

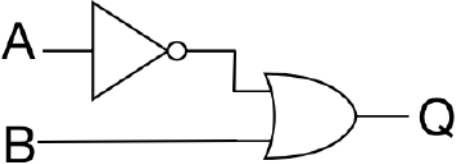
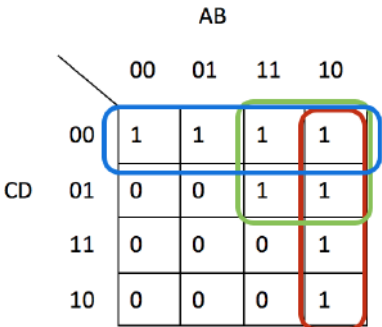
Mark Scheme

Question			Answer/Indicative content	Marks	Guidance																																																		
8			<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>X</th><th>Marking Guidance</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">1 Mark</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">1 Mark</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">1 Mark</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">1 Mark</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	A	B	C	D	X	Marking Guidance	0	0	0	0	0	1 Mark	0	0	1	0	1	0	1	0	0	0	1 Mark	0	1	1	0	1	1	0	0	0	0	1 Mark	1	0	1	0	1	1	1	0	1	1	1 Mark	1	1	1	1	0	4 AO2.2 (4)	Award 1 mark for each group of 4 1's / 0's.
A	B	C	D	X	Marking Guidance																																																		
0	0	0	0	0	1 Mark																																																		
0	0	1	0	1																																																			
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			Total	4																																																			
9		i	<table><tr><th>P</th><th>S</th><th>L</th></tr><tr><td>False</td><td>False</td><td>False</td></tr><tr><td>False</td><td>True</td><td>True</td></tr><tr><td>True</td><td>False</td><td>False</td></tr><tr><td>True</td><td>True</td><td>False</td></tr></table> 1 Mark for first 2 rows, 1 Mark for second 2 rows.	P	S	L	False	False	False	False	True	True	True	False	False	True	True	False	2 AO1.2	Accept any sensible representation of True or False <u>Examiner's Comments</u> Well answered by most candidates with some opting for a different representation of True / False in their response. These responses, where correct, were condoned but centres would best advise candidates to use the representations given in the context in future series.																																			
P	S	L																																																					
False	False	False																																																					
False	True	True																																																					
True	False	False																																																					
True	True	False																																																					
		ii	-P going into NOT Gate -S going into AND gate... -...NOT P going into AND gate, L coming out of it and no additional gates or connections. (1 per -, max 3)	3 AO3.1	 <u>Examiner's Comments</u> Generally, candidates responded well to this question, but some candidates used incorrect logic gate representations. Centres should remind candidates of the acceptable boolean algebra logic gate representations see specification appendix 5d.																																																		
			Total	5																																																			

Mark Scheme

Question			Answer/Indicative content	Marks	Guidance																																				
10			<table><tr><td>A</td><td>B</td><td>C</td><td>Q</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> First 4 rows correct 1 mark Last 4 rows correct 1 mark	A	B	C	Q	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0	0	1	1	1	1	2 (AO2.2)	<u>Examiner's Comments</u> Most candidates achieved both marks on this question. The presentation of some responses made it difficult to determine if the candidate was offering a zero or a one. Centres should encourage candidates to rewrite their response if they have overwritten a zero with a one and vice versa.
A	B	C	Q																																						
0	0	0	1																																						
0	0	1	1																																						
0	1	0	1																																						
0	1	1	1																																						
1	0	0	1																																						
1	0	1	1																																						
1	1	0	0																																						
1	1	1	1																																						
			Total	2																																					

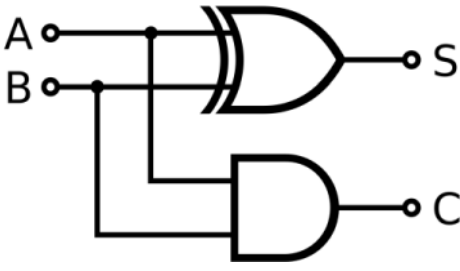
Mark Scheme

Question		Answer/Indicative content	Marks	Guidance
11	a	 - A going into NOT gate. - B and NOT A going into OR gate (and Q coming out of it) (1 Mark per -, Max 2)	2 (AO1.2)	Examiner's Comments Most candidates achieved both the available marks on this question.
	b	- Groups correctly identified (with no further groups). - Answer includes $\neg C \wedge \neg D$ - Answer includes $\neg C \wedge \neg D$ - Answer includes $\neg C \wedge \neg D$ - All three sections joined with $\wedge$s in any order but with no further sections. E.g. $(A \wedge \neg B) \vee (A \wedge \neg C) \vee (\neg C \wedge \neg D)$ The brackets aren't necessary (1 Mark per -, Max 5)	5 (AO1.2)	 Examiner's Comments The question required candidates to find the Boolean expression represented in the Karnaugh Map. Most candidates achieved a mark for showing the correct groupings on the map. Many went on to achieve some marks for the resultant expression. Some candidates specified NOT(C AND D) instead of NOT C AND NOT D evidently assuming the expressions are the same.
Total			7	

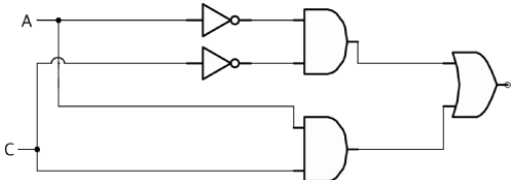
Mark Scheme

Question			Answer/Indicative content	Marks	Guidance																																																						
12	a		$Q = (A \wedge B) \vee (C \wedge D)$ 1 mark for $(A \wedge B)$ 1 mark for $(C \wedge D)$ 1 mark for the $\vee$ joining the two parts.	3 (AO1.2)	Accept $(C \wedge D) \vee (A \wedge B)$ Accept $(B \wedge A)$ instead of $(A \wedge B)$ Accept $(D \wedge C)$ instead of $(C \wedge D)$ Accept alternative notations (e.g. +/ . OR / AND) Accept AB as $(A.B)$ and CD as $(C.D)$ Accept answers without brackets Examiner's Comments In general, most candidates achieved all of the available marks in these questions.																																																						
	b	i	<table border="1"> <thead> <tr> <th>E</th><th>F</th><th>G</th><th>$(E \wedge F)$</th><th>$(E \wedge G)$</th><th>$(E \wedge F) \vee (E \wedge G)$</th></tr> </thead> <tbody> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </tbody> </table> 1 mark for each of the pairs of rows.	E	F	G	$(E \wedge F)$	$(E \wedge G)$	$(E \wedge F) \vee (E \wedge G)$	1	1	1	1	1	1	1	1	0	1	0	1	1	0	1	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	4 (AO1.2)	
E	F	G	$(E \wedge F)$	$(E \wedge G)$	$(E \wedge F) \vee (E \wedge G)$																																																						
1	1	1	1	1	1																																																						
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0	1	0	0	0	0																																																						
0	0	1	0	0	0																																																						
0	0	0	0	0	0																																																						
		ii	$(F \vee G) \wedge E$ One mark for the $(F \vee G)$ One mark for the $\wedge E$	2 (AO2.2)	Accept: $(G \vee F) \wedge E$ $E \wedge (F \vee G)$ $E \wedge (G \vee F)$ Examiner's Comments In general, most candidates achieved all of the available marks in these questions.																																																						
			Total	9																																																							

Mark Scheme

Question		Answer/Indicative content	Marks	Guidance
13	a	 XOR Gate (1) AND Gate (1) Correct connections and no additional gates (1)	3 (AO1,1)	Examiner's Comments Most candidates scored well on these questions demonstrating their understanding of logic gate circuits. Some candidates simplified the circuit in part b) which achieved full marks provided the resultant circuit gave the same output.

Mark Scheme

Question			Answer/Indicative content	Marks	Guidance
	b		– Correctly identified groups on Karnaugh map / Correct boolean statement.(1) – NOT A AND NOT C Gates (1) – A AND C gates (1) – Both sets of gates joined by OR gate (with no other gates used). (1)	4 (AO2.2)	AB 00 01 11 10 00 1 1 0 0 CD 01 1 1 0 0 11 0 0 1 1 10 0 0 1 1 $(\neg A \wedge \neg C) \vee (A \wedge C)$ Or equivalent.  Or equivalent. Examiner's Comments Most candidates scored well on these questions demonstrating their understanding of logic gate circuits. Some candidates simplified the circuit in part b) which achieved full marks provided the resultant circuit gave the same output.
			Total	7	